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A Review on Quaternary High Performance Arithmetic Unit Design

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ABSTRACT: Multiple Valued Logic (MVL) has been gaining popularity and practical applications. In addition to the standard MVL benefits, quaternary logic offers the benefit of easy interfacing to binary logic due to the fact that the radix $4=2^2$ allows for simple encoding/decoding circuits. Quaternary cells based on the Supplementary Symmetrical Logic Circuit Structure (SUSLOC) are modeled and used for adder circuit structures. Interconnections play a crucial role in modern FPGAs, because they dominate delay, power and area. MVL allows the reduction of the number of interconnections in the circuit, hence can serve as a mean to effectively place restrictions on the impact of interconnections. Quaternary implementation overcomes previous proposed techniques with simple and efficient CMOS structures.

KEYWORDS: MVL-Multi Valued Logic, SUSLOC-Supplementary Symmetrical Logic Circuit Structure, QSD-Quaternary Signed Digit, VHDL.

I. INTRODUCTION

As the technology is evolving the number of devices accommodated on the IC goes on increasing because of this many problems arise. The interconnection inside and outside of the integrated circuits becoming very complicated and area occupied by the interconnect goes on increasing. Inappropriate routing results in a large chip size and hence causes crosstalk and timing problems. This problem has the highest priority in deep submicron designs. The solution for this problem is to use quaternary number system. In integrated circuit about 70 percentage of the area is occupied by the interconnection which occupy the large portion of the physical area even when it is not in use. The interconnections will be more efficient when more than two levels of logics are injected into the single wire, this concept is known as multiple value logic (MVL) concept. This multi value logic concept improves overall information efficiency. The routing area for quaternary logic design is two times smaller than the corresponding binary logic system. The arithmetic operations performed on quaternary number system are addition, subtraction and multiplication. The speed of operation of digital processors, computers are depending on the arithmetic unit. The quaternary arithmetic unit performs carry free addition hence no carry is generated at the output and because of this quaternary arithmetic unit is faster as compared to binary arithmetic unit. The benefits of multi value logic implementation technique were considered for application in the reconfigurable domain. A new lookup table (LUT) structure was proposed where the information is represented by quaternary values. A new quaternary logic cell was presented and a result demonstrates interesting area and power reductions in comparison to equivalent binary structures. Some of the benefits of multi value logic include increased data density, reduced dynamic power dissipation, increased computational ability. The drawback of this multi value logic implementations are that they either based on current mode devices or demands extra steps in the fabrication process.

II. RELATED WORK

In quaternary arithmetic unit which is made up of radix 4 system, the arithmetic operations performed are addition, subtraction and multiplication. The addition performed here is carry free addition so the speed of operation is very fast in comparison with standard arithmetic unit [1]. In this paper standard CMOS design is used to design arithmetic unit.

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Clock boosting technique is used to optimize the switches resistance and power consumption. In CMOS technology the full adder prototype based on LUT works at 100 MHz and it consumes power of 122 μ W [2]. The result shows efficiency of the proposed design. In quaternary arithmetic unit the number of input bits are independent, the final result we get has the constant delay this delay is not depend on number of input bits i.e. when the input is of 4 bit, 8 bit, 16 bit, 32 bit and more, the delay is same. So for the higher number of bits and complex circuit the delay is independent. The current mode circuit allow successful improvement in terms of area. In the voltage mode look up table the major problem is power dissipation and it uses standard CMOS process, the threshold voltage is different for different transistors hence more number of fabrication steps are required and this is very expensive.

III. METHODOLOGY

In digital systems like computers and digital signal processors arithmetic operation plays a very important role. Arithmetic operations based on binary number system include problems like higher propagation delay, circuit complexity. When the number of bits increases the hardware also increases which means complexity goes on increasing. According to moor's law the number of transistors in an integrated circuit has doubled approximately every two years hence in integrated circuits the number of components goes on increasing because of this interconnects increases, nearly 70 percent area of the chip is occupied by interconnections. This problem can be overcome by multiple value logic concepts. The QSD numbers are both positive and negative numbers.

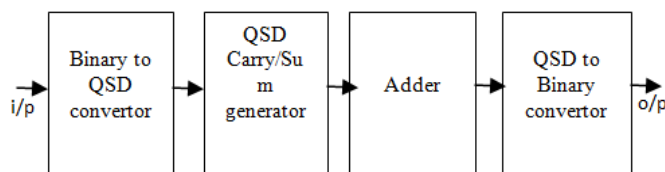


Fig. 1. Block Diagram of QSD Arithmetic Unit

The input to the system is binary numbers, the binary to quaternary conversion unit converts binary input to the quaternary and then it proceeds towards the quaternary arithmetic unit. The quaternary arithmetic unit performs the arithmetic operations like carry free addition, borrow free subtraction, multiplication on the input data. Finally the output of the quaternary arithmetic unit is given to the quaternary to binary conversion unit to convert it back to binary form.

A. SUSLOC Design

There are so many methods have been proposed in the recent years to realise the MVL circuit. The MVL circuits are of three type's i.e. current mode circuits, voltage mode circuits and mixed mode circuits. In the current mode circuit the power consumption is very high as compared to voltage mode circuit because of the constant current flow through the circuit. In voltage mode circuits the power is consumed only during logic level switching with any additional leakage current which is present in the circuitry hence the power consumption in voltage mode circuit is less in comparison with current mode circuit. Supplementary symmetry logic circuit is a self-sustaining and consistent circuit architecture which is proposed and patented. This proposed circuit allows the use of readily available circuit element to construct logic circuits based on any radix number system. Three requirements must be met by the circuit structure to design and fabricate MVL circuits.

- There must be 'r' different sources of power available including ground with each source of power representing of 'r' different logic levels.
- There must be one controllable path, or branch from a source of power to an output terminal of the circuit per output logic level.
- Only one controllable path or branch conducts from a source of power to an output terminal per input logic level, contiguous group of input logic levels or a unique combination of input logic levels.

The design rules and definitions of SUSLOC structure must meet all the above three requirements.

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IV. QUATERNARY CONVERSION CIRCUITS

In multi value logic down literal circuit (DLC) is used to divide multi value inputs to the binary state at an arbitrary threshold. Down literal circuit is made up of CMOS inverter by changing the threshold voltage of PMOS and NMOS transistors. One of the objectives of quaternary circuit is optimization, the optimization is achieved by minimizing the number of gates and hence chip size gets reduced. Figure 2 shows the down literal circuit (DLC).

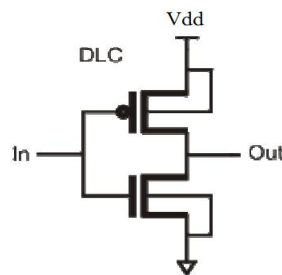


Fig. 2. Down Literal Circuit

The circuit can be easily fabricated by standard CMOS process, instead of the multi-level ion implantation applied in the conventional circuit. It has a variable threshold voltage by way of controlling only two bias voltages. Its noise margin and switching sensitivity are greater than those of variable-threshold C-VMOS inverter.

A. Binary to Quaternary Converter

Figure 3 shows the binary to quaternary converter circuit. In this circuit two DLCs are used, the LSB and MSB are given to these DLCs. The MOSFETs used in this circuit works on different threshold voltages. DLC circuits used here are similar to the CMOS inverter circuit except there threshold values.

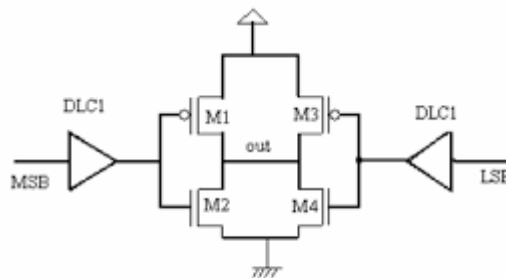


Fig. 3. Binary to Quaternary Converter Circuit

B. Quaternary to Binary Converter

Quaternary to binary converter circuit requires three down literal circuits DLC1, DLC2, DLC3 and the 2:1 multiplexer. The DLC used in the circuit works on different threshold voltages. The input is given to three DLC circuits and the output we get is in the inverted form hence we need to pass this output through the inverter circuit and finally we get the actual output. The quaternary to binary converter circuit is shown in the figure 4.

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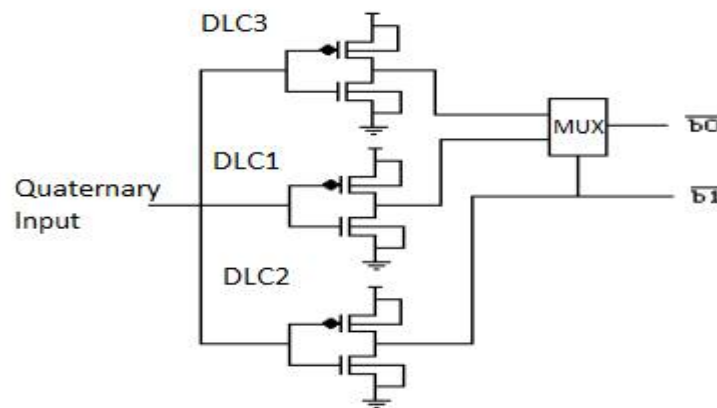


Fig. 4. Quaternary to Binary Converter Circuit

V. CONCLUSION

In this paper SUSLOC circuit structure is used to implement quaternary circuits. The conversion of binary to quaternary circuit is feasible and efficient in terms of power consumption and speed while being implemented in a standard CMOS technology. As technologies are becoming more complex, multi valued logic (MVL) will be the future of circuit design. Since the research is still in initial stage on MVL the work is fundamental. When hardware implementation using MVL circuits is famous and more exposed to companies then one day MVL will surely turn over the binary logic. The advantages of lower power, higher performance, and reduced interconnect congestion motivate the use of quaternary circuits in a wide variety of applications.

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